ABSTRACT

A method for fabricating a high-density array of crown capacitors with increased capacitance while reducing process damage to the bottom electrodes is achieved. The process is particularly useful for crown capacitors for future DRAM circuits with minimum feature sizes of 0.18 micrometer or less. A conformal conducting layer is deposited over trenches in an interlevel dielectric (ILD) layer, and is polished back to form capacitor bottom electrodes. A novel photoresist mask and etching are then used to pattern the ILD layer to provide a protective interlevel dielectric structure between capacitors. The protective structures prevent damage to the bottom electrodes during subsequent processing. The etching also exposes portions of the outer surface of bottom electrodes for increased capacitance (> 50%). In a first embodiment the ILD structure is formed between pairs of adjacent bottom electrodes, and in a second embodiment the ILD structure is formed between four adjacent bottom electrodes.